

<b>Notice of References Cited</b>	Application/Control No. 10/666,031	Applicant(s)/Patent Under Reexamination AIPPERSPACH ET AL.	
	Examiner Shelly A. Chase	Art Unit 2133	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,490,155	02-1996	Abdoo et al.	714/763
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Nakamura et al., Giga-bit DRAM cells with low capacitance and low resistance bit-lines on buried MOSFET's and capacitors by using bonded SOI technology Reversed stacked capacitor (RSTC) cells, 1995, IEEE, pg. 35.4.1-35.4.4.
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.